



Computational Diagnostics, Inc.
Leaders in Clinical Neurophysiology

Brain-Implantable Computing Platform (BICP)

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BICP - Motivation

Advances in nanoelectronics coupled with our growing understanding of human brain function has enabled neuroscientists to conceive of brain implantable computational systems to:

- repair damaged portions of the brain
- enhance neural capabilities beyond our natural capabilities

Examples are:

- sense the onset of seizures and suppress them via implanted deep brain stimulators.
- interface the brain with neuroprosthesis or disabled limbs.
- augment brain memory function by replacing damaged hippocampal structures.



BICP - Vision

We envision a BICP which is an implantable distributed computing system, consisting of millimeter scale computational elements, interfaced with brain sensors and actuators, which will communicate wirelessly between both implanted elements and the outside environment and which will wirelessly draw mWatt power.

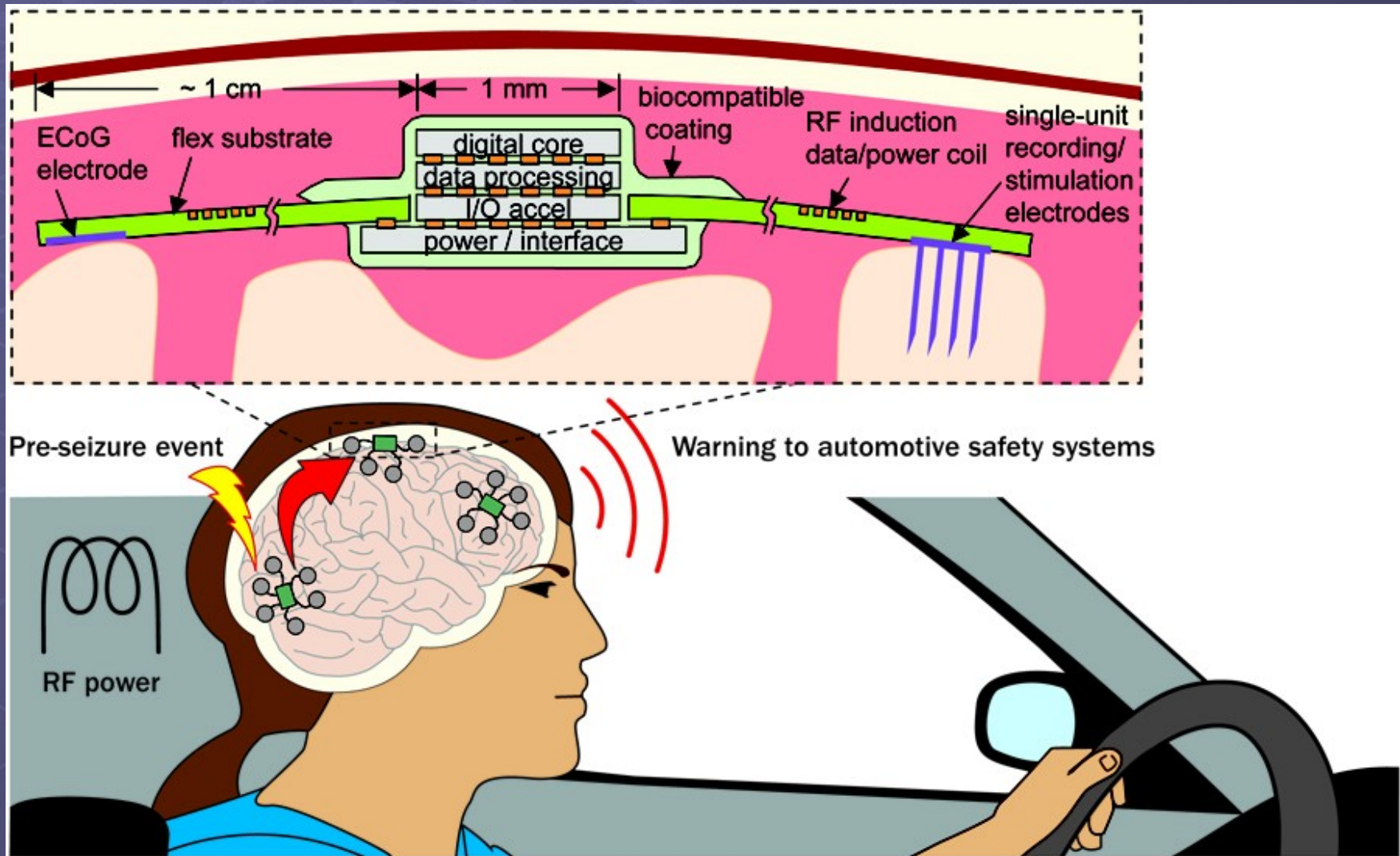
The goal is to develop a technology path which would be useful many years into the future.



BICP - Requirements

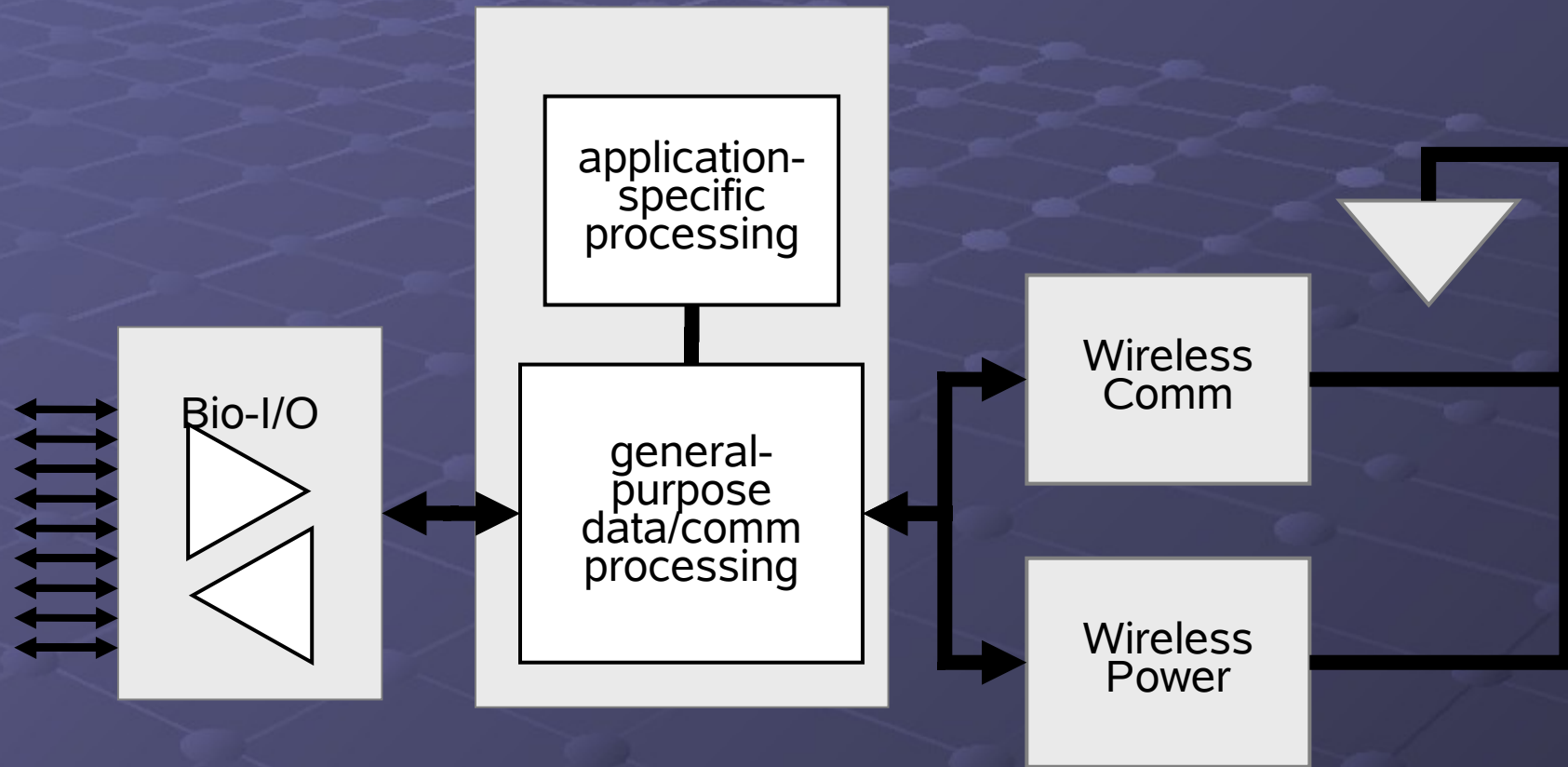
- Support for a wide range of neuroscience applications via a customizable distributed computational architecture base on nanoelectronics.
- Highly energy efficient operation to fit within a severely constrained power envelope.
- Sustainable wire-free delivery of milliwatt-level power.
- Minimal thermal interface to surrounding tissues.
- Efficient wireless communication between elements of the distributed system and to external devices.
- Novel sensors to interface with brain tissue.
- Cubic millimeter form-factor with bio-compatible packaging for fully-enclosed implantation.
- Secure and reliable operation over a multi-year timeframe.

BICP – Application Seizure Detection and Control with DBS





BICP – Major Subsystems





BICP – Technology Assessment

| | | Power (mW) | Bandwidth SPS=sample/sec | Processing (MOP/sec) | Storage (Mbits) | Comm Methods | Energy Lifetime |
|---------------------------------|----------------------|--|---------------------------|----------------------|--------------------------------|---------------------|-----------------------------------|
| State-of-the-Art Brain Implants | Neural Recording | 10-20 | 100 channel, 100 kSPS | N/A | N/A | high rate inductive | inductive link |
| | Nerve Stimulation | 0.2-1 | 10 SPS | minimal | minimal | wired or inductive | 1-5 year battery |
| Projected Demands | Low-End BCI | sense/decode= 5-10; stimulation= 20-30 burst | 32-64 channel, 1 kSPS | 1 - 1000 | up to 1000 | wireless telemetry | 10+ yr lifetime; wire-free rechg. |
| | High-End BCI | | 100 channel, 50 kSPS | 1 -1000 | up to 1000 | | |
| | Epilepsy | detect=1-5 arrest=10-30 | 4-64 channel, 1-20 kSPS | 10-100 | 10-1000 | | |
| | Monitor & Rx Deliver | monitor <1 actuate >50 | < 5 channel, 1-100 SPS | < 1 | 1-10 | | |
| BICP Target | | 1- 2 | 4-100 channel, 1-100 kSPS | Up to 3.2 | up to 1000 per mm ³ | wireless | wire-free |



BICP - Computation

Nanocomputing elements in the future.

Performance, power usage and area of digital computation elements are highly dependent on process technologies.

Current state of the art of 45 nm technologies and predicted capabilities of 22 nm technologies five years out.

Current Questions:

- What amount of circuitry can fit into 1mm^3 ?
- What computation rate can be sustained with 1 mW of power?



BICP – Density and Performance Projections

| | 2008 (45nm) 1mm x 1mm die | 2014 (22nm) 1mm x 1mm die | 2014 (22nm) 5 chip stack |
|-------------|------------------------------|------------------------------|-----------------------------|
| Logic gates | 400k | 1.6M | 8.0M |
| SRAM | 2Mb | 8Mb | 40Mb |
| DRAM | 25Mb | 100Mb | 500Mb |
| FLASH SLC | 50Mb | 200Mb | 1Gb |

| MOPS per 1mW | 2008 (45nm) | 2014 (22nm) |
|-------------------------|--------------------|--------------------|
| ASIC | 800 | 3200 |
| ASP | 16 | 64 |
| CPU | 0.2 | 0.8 |

Consider Moore's Law 50 years out – increased capability 2^{25}



BCIP – Computational Considerations

Architecture

- High energy efficiency – customized vs general purpose designs.
- Domain-specific architecture – hardware functional blocks.
- Custom hardware accelerator modules.
- Run-time dynamic reconfigurability.

VLSI Implementation

- Specialized low-power techniques.
- Trans-threshold circuits.
- Sloppy logic components – imperfect operations.



BICP - Communications Volume Conduction

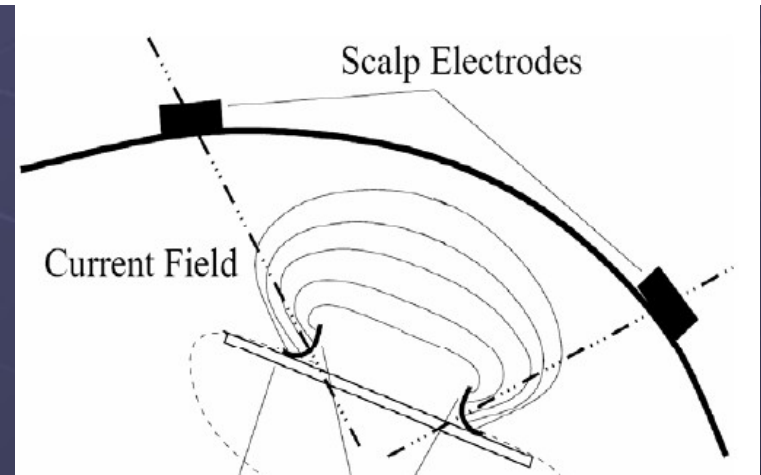
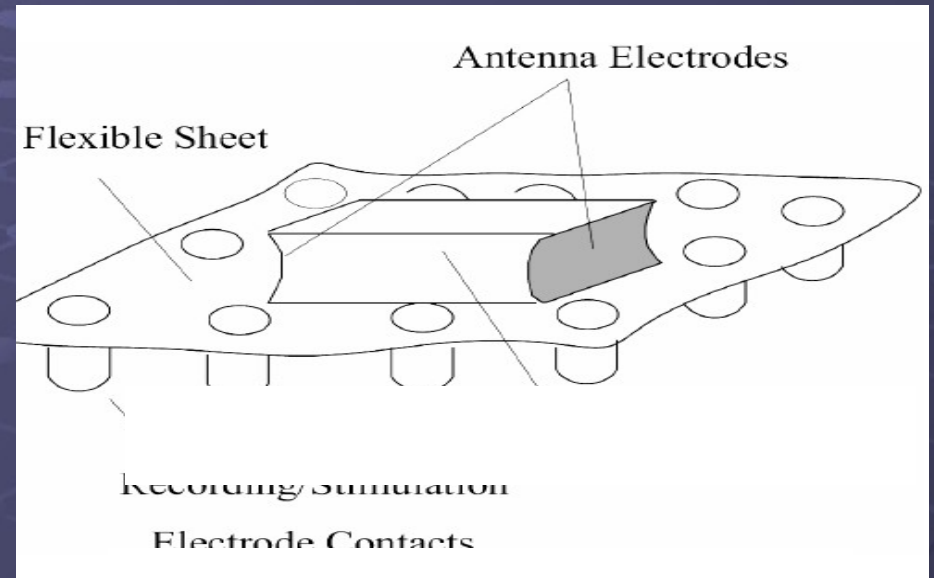
Human body is a natural conductor.

Can be used to pass information (or power).

Electrostatic theory provides basis.

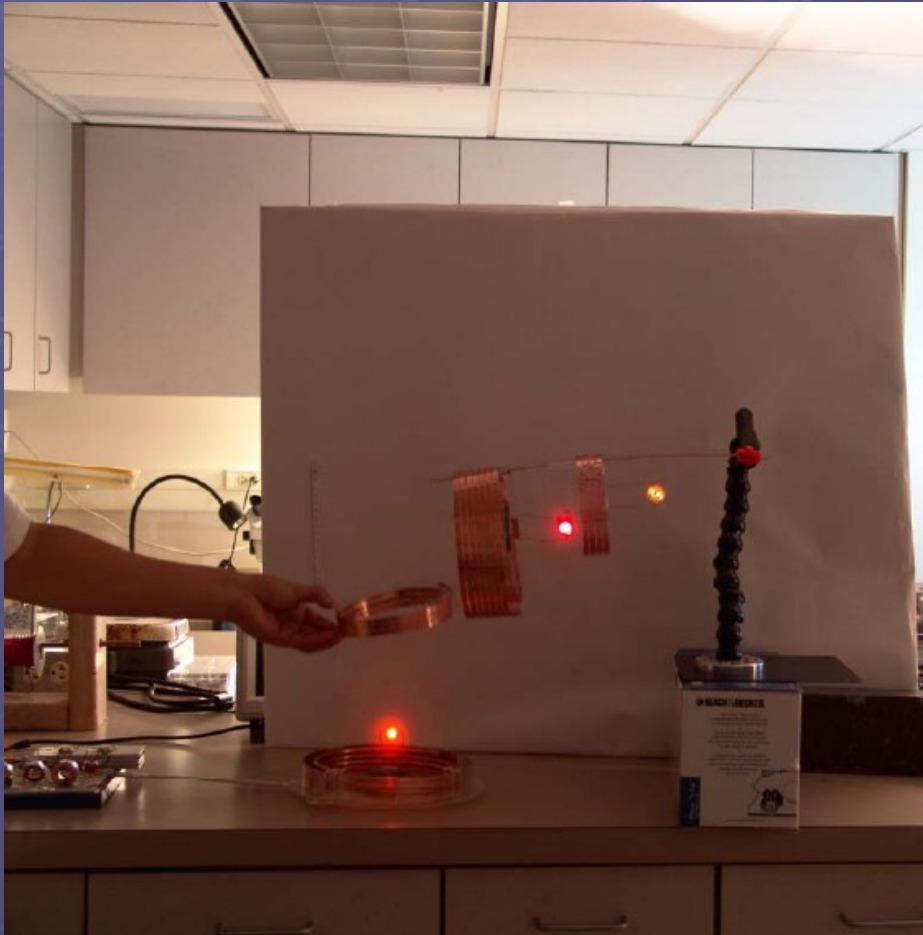
Advantages

- Low power consumption
- No shielding effects
- Simple circuits
- Small size/mass
- High security
- 10 Mbps data rate





BCIP – Energy Thin Film Power Transfer Cell

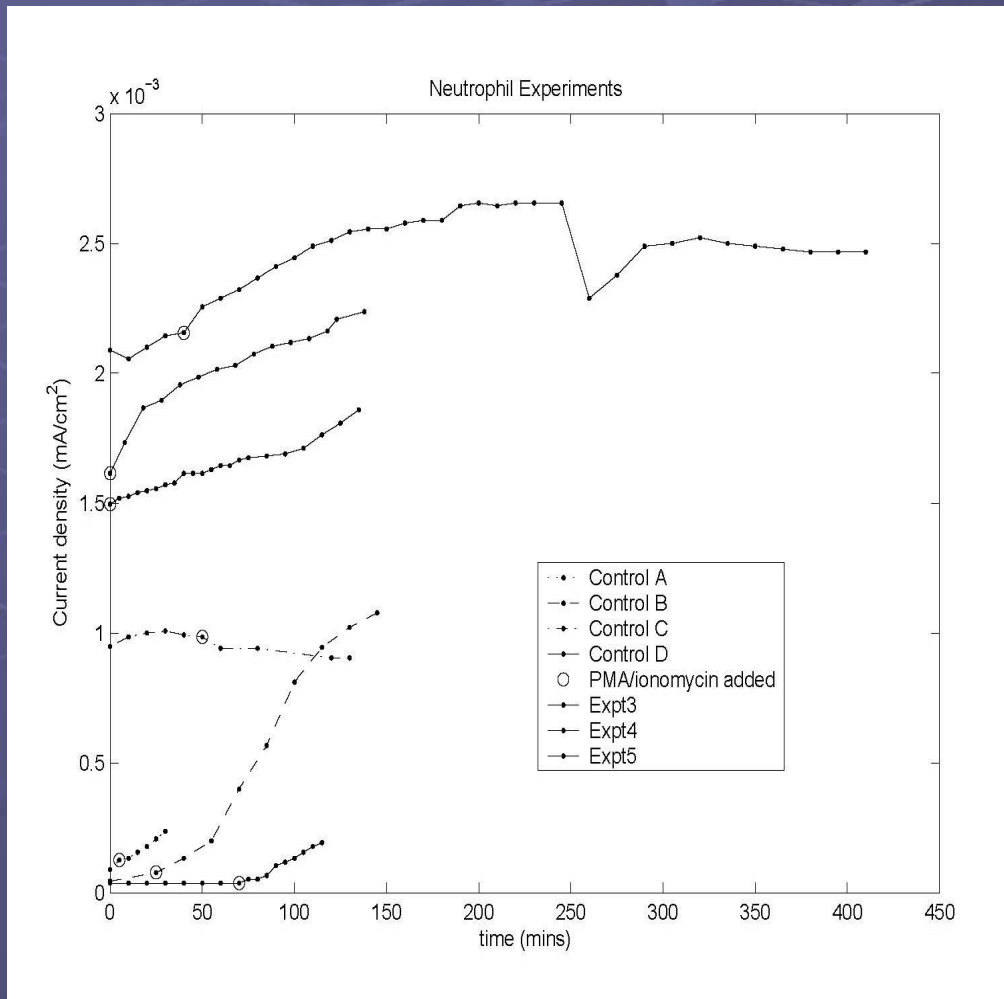


- Magnetic resonance is key.
- Differs from RF coupling commonly used.
- Electric fields are trapped within capacitors.
- Thin film designs.
- Design is a LC resonator.
- Capacitance of the LC tank is high and stable.
- Magnetic fields interact weakly with biological tissues.
- May also be used as communication channel.



BCIP-Energy Energy from Human Neutrophils

- Proton exchange membrane fuel cells.
- Current densities between 0.9 and 1.6 $\mu\text{A}/\text{cm}^2$.
- OPen circuit voltages between 83 and 102 mv.
- Serotonin has been identified as being released from WBCs.
- Serotonin is the likely source of the electrons captured in the fuel cell.
- Same mechanism appears to work with microglia.





BICP - Algorithms

Signal Processing Algorithms must be re-thought:

- Stringent power/size limits.
- Plasticity of the brain
 - neuron signals - non-stationary
 - brain function – varies dynamically over space and time
- Algorithms must be flexibly parameterized
 - trade-offs between – allow for graceful degradation
 - accuracy
 - power
 - performance metrics
- Development of algorithms must be co-optimized with design of processor.



BICP – Brain Interface

Different applications – different types of signal acquisition

- Integrated natively onto the BICP
 - ADCs
 - DACs
 - Sparse data sampling methods
 - Amplitude quantization instead of time quantization
 - Discrete amplitude – continuous time
 - Signal conditioning
 - Communication
- Nanoscale CMOS analog devices
- Hybrid analog/digital approaches



BICP – Thermal Management

- Need to maintain an operational temperature.
- Heat generated must be transferred to and absorbed in the surrounding tissue.
- But exposure to above normal temperatures in the brain for extended periods of time be harmful.
- Lower power consumption does not guarantee less thermal injury.
- Power density drives localized temperature distribution.
- Thus the power density must be appropriately designed and controlled.
- Plan to use thermal sensors to drive a power management algorithm that conserves power and energy, bounds the thermal dose to the tissues, and meets the application performance requirements.



BICP – Reliability and Security

A system malfunction or failure is highly undesirable.

Effort is being placed on:

- Low-overhead techniques for reliable computing.
- Low-overhead techniques for secure integrated circuits with extensions to the ultra-low power operating domain of the BICP.
- Self-test for early wear-out detection.

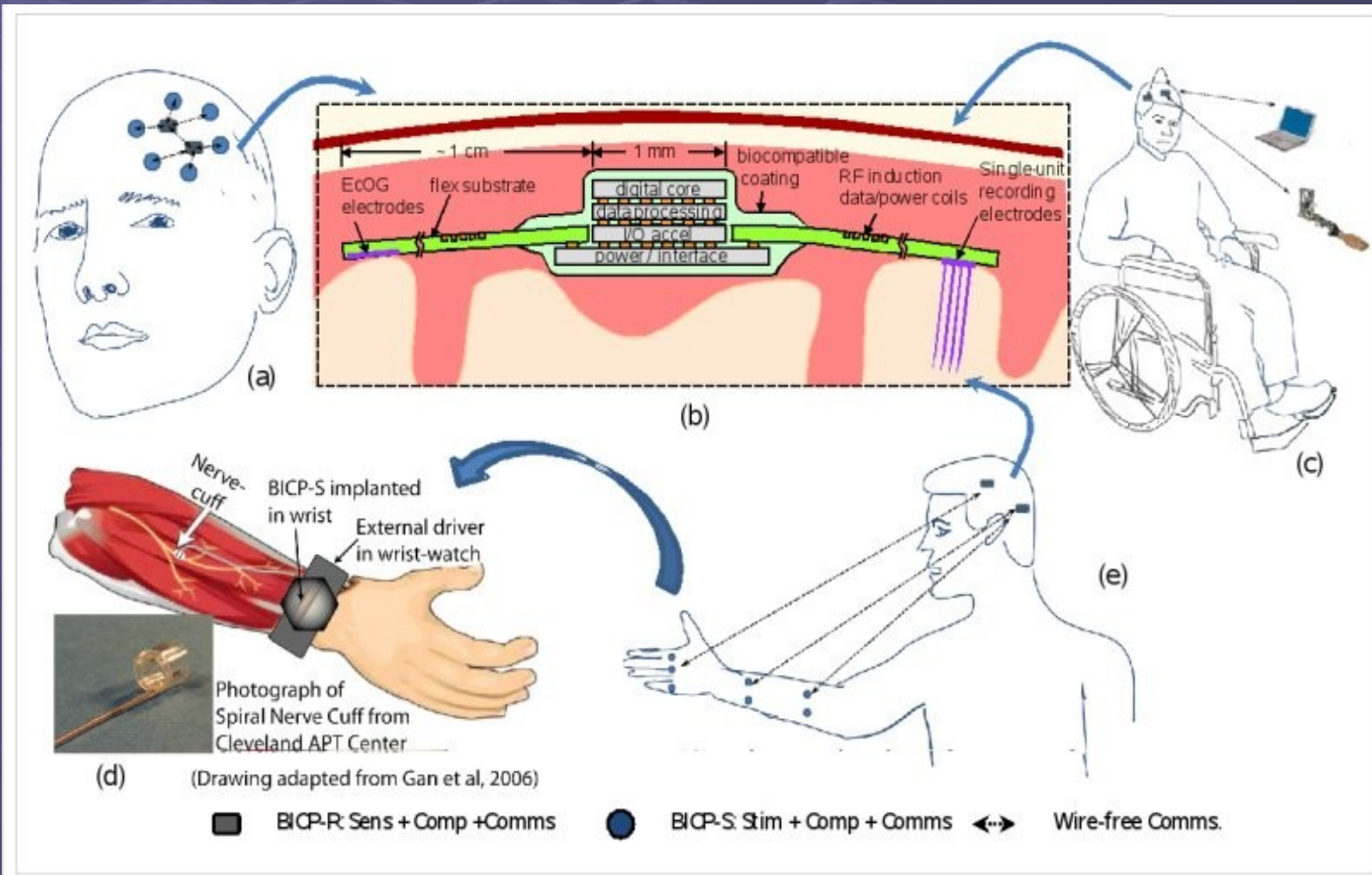


BICP - Packaging

- Low Profile (< 1mm) over cortical surface.
- Move with the brain (chronic applications).
- 3-D BICP chip stack and probes will be interconnected with ultralexible polyimide cabling or parlyene flex circuit boards.
- Coil or x-antennas printed directly on the flex board.
- Auxiliary components (Schottky diodes and capacitors) bonded directly on the flex board.
- BICP is a set of stacked chips
 - Probes, antenna, and capacitors on flex board.
- BICP sealed with bio-compatible material
 - Prevent fluids from seeping in and onto connections



BCIP – Testbeds Therapeutic and Functional Electrical Stimulation





BICP - Discussion

To accomplish our objectives we are rethinking the entire systems design stack, from application algorithms to implementation substrate.

Our BICP will be the first brain-implantable device to demonstrate significant computational resources within the implant itself.

The dramatic increase in computational capability of the implant will be a disruptive technology shift for both basic and clinical neuroscience.